

# PLL tone decoder IC

## BA1604 / BA1604F

The BA1604 and BA1604F are tone decoder ICs that enable the frequency to be selected in precise detail, using a PLL system. These ICs are configured of a PLL circuit, a detection circuit, a voltage comparator circuit and an output logic drive circuit.

When the input signal is within the transmission range of the circuit, PLL is synchronized (locked) to the input signal. At this point, the output voltage of the decoder drops, and the change turns on the transistors for the voltage comparator and output logic drive circuits. A load of up to 100mA can be driven. The center frequency ( $f_0$ ) of the decoder is set by the mobile oscillation frequency of the current control oscillator. This frequency is determined by selecting a CR connected to Pins 5 and 6.

### ● Applications

Telephones

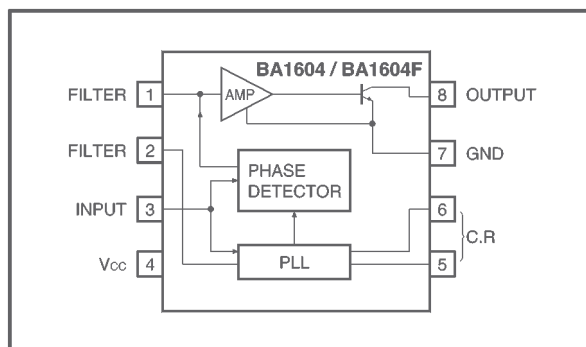
Data communication systems

Remote control systems

### ● Features

- 1) The detection bandwidth can be varied independently between 0 and 14%.
- 2) The output circuit can withstand a load current of up to 100mA, and is directly coupled to the logic circuit.
- 3) The center frequency offers a high level of stability.
- 4) High out-of-band signal and noise rejection capability.
- 5) Frequency can be changed over a range of 20 : 1 using an external resistor.
- 6) Compatible with EXAR XR-567 and Signetics NE567.

### ● Block diagram



## ● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>CC</sub>	9	V
Power dissipation	BA1604	300*1	mW
	BA1604F	350*2	
Operating temperature	T <sub>opr</sub>	-10~+75	°C
Storage temperature	T <sub>stg</sub>	-55~+125	°C

\*1 Reduced by 3 mW for each increase in Ta of 1°C over 25°C.

\*2 Reduced by 3.5 mW for each increase in Ta of 1°C over 25°C.

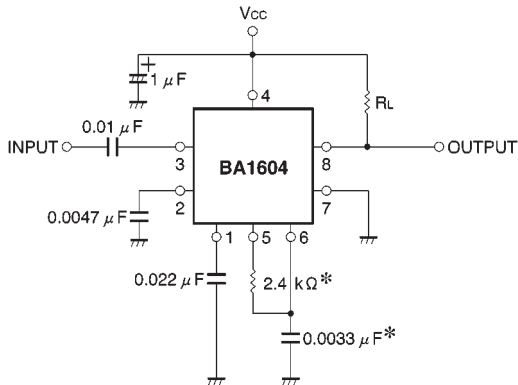
## ● Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V <sub>CC</sub>	4.75	6.0	9.0	V

● Electrical characteristics (unless otherwise noted, Ta=25°C, V<sub>CC</sub>=5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current 1	I <sub>Q-1</sub>	—	6.0	10	mA	R <sub>L</sub> =20kΩ, detector OFF
Quiescent current 2	I <sub>Q-2</sub>	—	10	15	mA	R <sub>L</sub> =20kΩ, detector ON
Output voltage	V <sub>OUT</sub>	—	—	15	V	—
Input voltage	V <sub>IN</sub>	-10	—	V <sub>CC</sub> +0.5	V	—
Frequency stability	Δf <sub>OT</sub>	—	±60	—	ppm / °C	—
Frequency stability	Δf <sub>OV</sub>	—	0.5	2.0	% / V	—
Maximum detection bandwidth	W <sub>Max.</sub>	10	14	18	% of f <sub>0</sub>	f <sub>0</sub> =100kHz
Maximum detection bandwidth skew	ΔW <sub>Max.</sub>	—	—	3	% of f <sub>0</sub>	—
Change in maximum detection bandwidth	ΔW <sub>t</sub>	—	±0.1	—	% / °C	V <sub>IN</sub> =300mV <sub>rms</sub>
Change in maximum detection bandwidth	ΔW <sub>v</sub>	—	±2	—	% / V	V <sub>IN</sub> =300mV <sub>rms</sub>
Input resistance	R <sub>IN</sub>	—	20	—	kΩ	—
Minimum input voltage at detector ON	D <sub>ON</sub>	—	20	25	mV <sub>rms</sub>	I <sub>L</sub> =100mA, f <sub>i</sub> =f <sub>0</sub>
Maximum input voltage at detector OFF	D <sub>OFF</sub>	10	15	—	mV <sub>rms</sub>	I <sub>L</sub> =100mA, f <sub>i</sub> =f <sub>0</sub>
2-signal selection ratio	V <sub>IR</sub>	—	6	—	dB	In-band/out-of-band signals
Minimum input signal-to-wide-band noise ratio	R	—	6	—	dB	B <sub>n</sub> =140kHz
Output saturation voltage 1	V <sub>sat-1</sub>	—	0.2	0.4	V	I <sub>L</sub> =30mA, V <sub>IN</sub> =25mV <sub>rms</sub>
Output saturation voltage 2	V <sub>sat-2</sub>	—	0.6	1.0	V	I <sub>L</sub> =100mA, V <sub>IN</sub> =25mV <sub>rms</sub>
Output leakage current	I <sub>L</sub>	—	0.01	25	μA	—
Maximum ON-OFF cycle	T <sub>Max.</sub>	—	f <sub>0</sub> /20	—	—	—
Output rise time	t <sub>H</sub>	—	150	—	ns	R <sub>L</sub> =50Ω
Output fall time	t <sub>L</sub>	—	30	—	ns	R <sub>L</sub> =50Ω

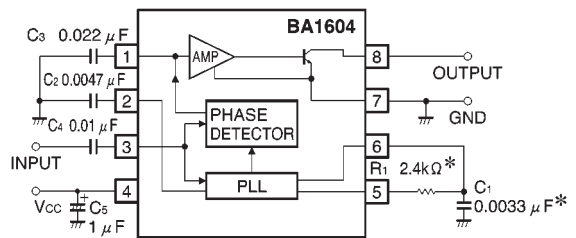
● Measurement circuit



\* Fine adjustment should be done until  $f_0 = 100$  kHz

Fig. 1

● Application example



\*  $C_1$  and  $R_1$  should be adjusted until  $f_0 = 100$  kHz

Fig. 2

● Attached components

(1)  $C_1$  and  $R_1$  : Setting  $f_0$

The center frequency ( $f_0$ ) is determined by the resistor  $R_1$  between Pins 5 and 6, and the capacitor  $C_1$  between Pin 6 and the ground. The constants at this point are determined as follows :

$$f_0 \doteq \frac{1}{C_1 R_1} \quad (\text{kHz}) \quad (C : \mu \text{ F}, R : \text{k}\Omega)$$

A rectangular-wave voltage is output at Pin 5; the peak-to-peak amplitude is between  $V_{CC}$  and 1.4 V, and the average DC value is  $V_{CC} / 2$ . This pin can drive a load resistance of up to 1k $\Omega$ . (The recommended value for  $R_1$ , however, is from 2k $\Omega$  to 20k $\Omega$ .)

A 1V peak-to-peak exponential function triangular wave with an average DC voltage level of  $V_{CC} / 2$  is output at Pin 6. Since loading this pin adversely affects both the duty cycle and the temperature stability of the oscillator, it must only be connected to a high-impedance load.

(2)  $C_2$  : Loop filter

Connected between Pin 2 and the ground,  $C_2$  functions as a low pass filter for the PLL circuit, and the time constant is determined by  $T_2 = R_2 C_2$  ( $R_2$  is the internal impedance for Pin 2, at 10 k $\Omega$ ). The value of  $C_2$  also determines the detection bandwidth. The voltage at Pin 2 varies linearly at 20mV / % of  $f_0$  over the range 0.95  $f_0$  to 1.05  $f_0$ .

(3)  $C_3$  : Output filter

Capacitor  $C_3$ , connected between Pin 1 and the ground, is used as a low pass filter to suppress out-of-band signals. The time constant  $T_3$  is determined by  $T_3 = R_3 C_3$  ( $R_3$  is the internal impedance for Pin 1, at 4.7k $\Omega$ ).

To prevent false detection of spurious signals, it is recommended that  $C_3 \geq 2 \times C_2$ . If  $C_3$  is made too large, however, this will increase the time required for voltage changes at Pin 1 to reach the threshold of the phase detector, thus slowing the response time.

(4)  $C_4$  : Input coupling capacitor

(5)  $C_5$  : Power supply filter capacitor

● Input and output pins

(1) Input : Pin 3

The input signal is applied through a coupling capacitor to Pin 3. Internal circuits set this pin to a DC potential of 2V with respect to the ground. The input impedance is approximately 20k $\Omega$ .

(2) Output : Pin 8

The output logic section has an internal power transistor with its collector connected to Pin 8. The load is connected between Pin 8 and  $V_{CC}$ . The transistor saturates when an in-band input signal is received, dropping the potential at Pin 8 to less than 1V (0.6V Typ.). The output can also drive a load connected to a separate supply voltage of up to 20V.

● Operation notes

When setting the central frequency, which is determined by the capacitor and resistor connected to pins 5 and 6 of this IC, it is recommended to connect a variable resistor between pins 5 and 6 and align the central frequency of each component in order to prevent shifting of the central frequency caused by fluctuations in the IC, capacitor, or resistor.

● Electrical characteristic curves

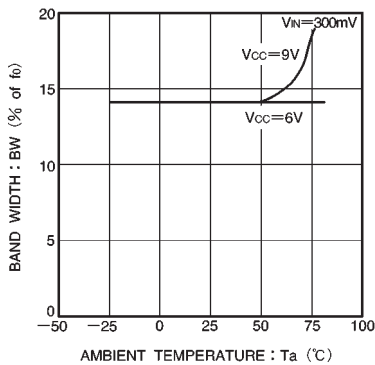


Fig. 3 Detection bandwidth vs. ambient temperature

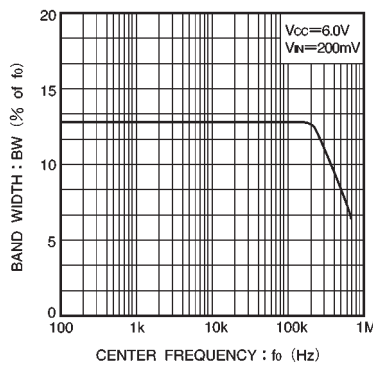


Fig. 4 Detection bandwidth vs. frequency

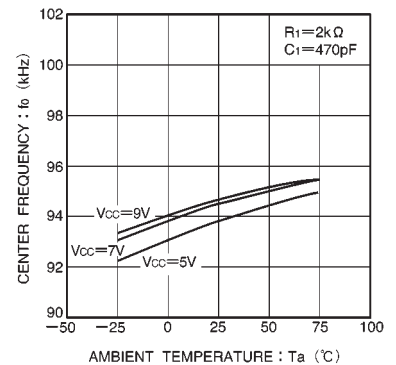


Fig. 5 Center frequency vs. ambient temperature

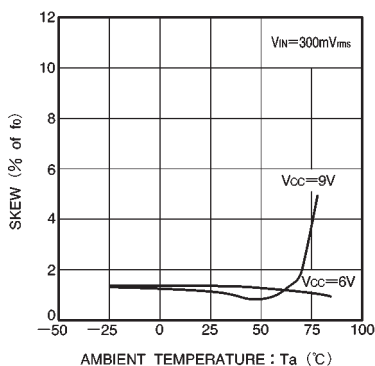


Fig. 6 Detection bandwidth skew vs. ambient temperature

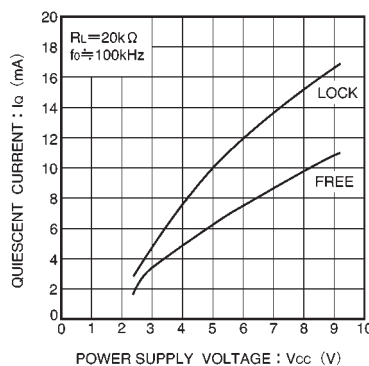


Fig. 7 Quiescent current vs. power supply voltage

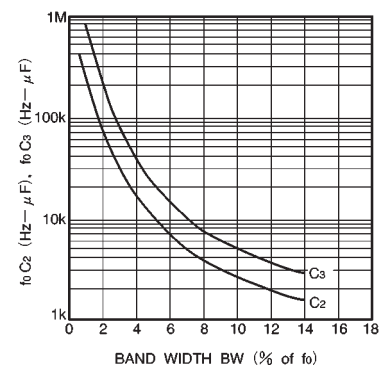


Fig. 8 Detection bandwidth based on C<sub>2</sub> and C<sub>3</sub>

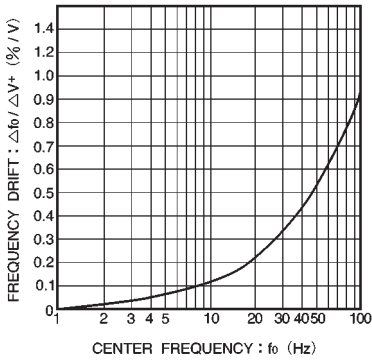


Fig. 9 Center frequency fluctuation based on power supply voltage vs. center frequency

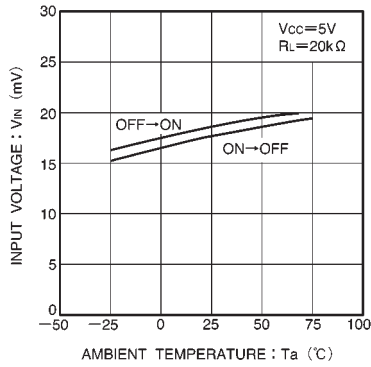


Fig. 10 Detector input sensitivity vs. ambient temperature

● External dimensions (Units: mm)

